UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,381	01/05/2001	Evelyn Duesterwald	10990963-1	5203

22879 7590 05/05/2004

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
YIGDALL, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2122	

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/755,381	DUESTERWALD ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,7-13 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-13 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is in reply to Applicant's response and amendment dated 19 February 2004. Claims 1-3, 7-13 and 17-20 remain pending.

Claim Objections

2. Claims 10 and 20 are objected to because of the following informalities: The claims are dependent upon claims that have been cancelled. Claim 10 is recited as "a method according to claim 4," and claim 20 is recited as "a computer readable medium according to claim 14." Claims 4 and 14 have been cancelled by the amendment. Appropriate correction is required. The claims have been interpreted as depending from claims 1 and 11, respectively.

Response to Arguments

3. Applicant's arguments filed 19 February 2004 have been fully considered but they are not persuasive.

4. In response to Applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant acknowledges the teaching of register masks by Click (see page 7). The register masks of Click, each of which have a plurality of bit positions, are used to indicate which registers are valid with respect to a variable (see Click, column 7, lines 50-53).

Applicant contends that the use of the register masks by Click has nothing to do with whether an instruction for assigning a register is possibly live for an exit of a code fragment, and

has nothing to do with whether or not a register is assigned in a code fragment before being read (see page 8, paragraphs 2 and 3).

However, the register masks of Click are considered only in combination with the dead code removal method disclosed by Srivastava. Srivastava discloses the first and second information as recited in the claims (see the explanations set forth below), but does not expressly disclose using register masks with this information. Nonetheless, Click discloses specifying how registers are to be used for procedure calls (see column 1, line 54 to column 2, line 7), using register masks (see column 8, lines 12-14). Because Srivastava uses the first and second information to correlate registers and instructions and to subsequently remove dead instructions (see column 10, lines 1-46), it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Srivastava and Click, and use register masks to support the correlation and dead code removal process.

Applicant also contends that the register masks of Click cannot correspond to both the first and second register masks recited in the claims, because the bits of the two register masks are set based on different criteria (see page 8, paragraph 3). However, as above, the teaching of register masks by Click is not relied upon in isolation, but is rather considered in combination with the dead code removal method disclosed by Srivastava.

Applicant further contends that the use of register mask intersection by Click, to determine the live range of a variable, has nothing to do with eliminating an instruction for assigning a register in the first code fragment if the positions corresponding to the register in the first and second register masks are both set (see page 8, paragraph 4). Again, as above, the teaching of register mask intersection by Click is considered only in combination with the dead

code removal method disclosed by Srivastava. Srivastava discloses eliminating dead instructions as recited in the claims (see the explanations set forth below), but does not expressly disclose using register masks, and therefore does not expressly disclose the condition in which positions corresponding to a register in the first and second register masks are both set. This condition is analogous to the intersection of register masks taught by Click.

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1, 7-11 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,999,737 to Srivastava in view of U.S. Pat. No. 6,408,433 to Click, Jr. et al. (hereinafter Click).

With respect to amended claim 1, Srivastava discloses a method for removing dead code in code fragments of a program (see column 3, lines 6-12), comprising:

(a) processing a first code fragment and storing first information generated during this processing indicative of whether an instruction for assigning a register in a first code fragment is possibly live (see column 9, lines 15-16, which shows analyzing a procedure or code fragment to determine the liveliness of registers used by the procedure, and column 10, lines 38-46, which shows storing liveliness information during the analysis), the first information including a pointer to each instruction for assigning a register that is possibly live for an exit of the first code fragment (see column 7, lines 38-46, which shows classifying the exit blocks of a procedure, and column 8, lines 6-12, which shows storing information for such blocks; see also column 10, lines

1-7, which shows that the stored information precisely conveys variable and register utilization in the program, which means that the information inherently comprises pointers to the instructions that use the registers).

Although Srivastava discloses using the first information to determine variable and register utilization across linked procedures (see column 10, lines 1-14) and to identify instructions that reference particular registers (see column 10, lines 28-31), Srivastava does not expressly disclose the limitation wherein the first information includes a first register mask having a plurality of positions, each position corresponding to a respective register, wherein a bit at a position is set if the respective register is assigned in an instruction pointed to by a pointer included in the first information.

However, Click discloses a register mask having a plurality of bit positions that are used to indicate which registers are associated with a particular variable (see column 7, lines 50-53). The register mask is used to describe register locations associated with a calling convention (see column 8, lines 12-14), which, in terms of dead code elimination, specifies how registers are to be used when procedures are called (see column 1, line 54 to column 2, line 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include, in the liveliness information of Srivastava, a register mask as taught by Click. The combination would have been obvious because the liveliness information of Srivastava is used to correlate registers and instructions (see Srivastava, column 10, lines 28-31), and the register mask of Click specifies such information as it applies to procedure calls (see Click, column 1, line 54 to column 2, line 7). Therefore, one of ordinary skill in the art would have been motivated to enhance the liveliness information of Srivastava with a register mask

specifying the use of registers in procedure calls, as taught by Click, for the purpose of providing further information from which to correlate registers and instructions.

Srivastava further discloses:

(b) processing a second code fragment and storing second information generated during this processing indicative of register usage (see column 9, lines 15-16, which shows analyzing a procedure or code fragment to determine the liveliness of registers used by the procedure, and column 10, lines 38-46, which shows analyzing a second procedure or code fragment and storing liveliness information during the analysis), the second information including information associated with an entry into the second code fragment (see column 7, lines 38-46, which shows classifying the entry blocks of a procedure, and column 8, lines 6-12, which shows storing information for such blocks);

(c) at a time when linking the exit from the first code fragment to the entry in the second code fragment, determining, by use of the first stored information associated with the exit and the second stored information associated with the entry, if an instruction in the first code fragment that assigns a register is a dead instruction (see column 3, lines 3-6, which shows performing liveliness analysis at link time, and FIG. 6, which shows linking the exit from a procedure to an entry in another procedure; see also column 10, lines 23-31, which shows determining whether instructions that reference a register are dead, and column 10, lines 38-46, which shows using the stored liveliness information to find dead instructions); and

(d) responsive to determination that an instruction is a dead instruction, eliminating the dead instruction (see column 10, lines 9-14, which shows removing dead code, and column 10, lines 23-31, which shows eliminating instructions determined to be dead instructions).

With respect to amended claim 7, although Srivastava discloses using the second information to determine variable and register utilization across linked procedures (see column 10, lines 1-14) and to identify instructions that reference particular registers (see column 10, lines 28-31), Srivastava does not expressly disclose the limitation wherein the second information associated with the entry includes a second register mask, the second register mask having a plurality of positions, each position corresponding to a respective register, wherein a bit at a position is set if the respective register is assigned in the second fragment before being read.

However, Click discloses a register mask having a plurality of bit positions that are used to indicate which registers are associated with a particular variable (see column 7, lines 50-53). The register mask is used to describe register locations associated with a calling convention (see column 8, lines 12-14), which, in terms of dead code elimination, specifies how registers are to be used when procedures are called (see column 1, line 54 to column 2, line 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include, in the liveliness information of Srivastava, a register mask as taught by Click. The combination would have been obvious because the liveliness information of Srivastava is used to correlate registers and instructions (see Srivastava, column 10, lines 28-31), and the register mask of Click specifies such information as it applies to procedure calls (see Click, column 1, line 54 to column 2, line 7). Therefore, one of ordinary skill in the art would have been motivated to enhance the liveliness information of Srivastava with a register mask specifying the use of registers in procedure calls, as taught by Click, for the purpose of providing further information from which to correlate registers and instructions.

With respect to original claim 8, although Srivastava discloses removing instructions that reference dead registers (see column 10, lines 28-31), Srivastava does not expressly disclose the limitation where said determining step comprises comparing corresponding positions of the first and second register masks, wherein said eliminating step includes eliminating an instruction for assigning a register in the first code fragment if the positions corresponding to the register in the first and second register masks are both set.

However, Click discloses finding the intersection of several register masks, i.e. finding corresponding set positions in several register masks, for the purpose of determining the live range of a variable, which is the range over which the variable is accessible by instructions (see column 8, lines 15-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the liveliness information of Srivastava by comparing register masks, as taught by Click, for the purpose of determining the range over which a variable is accessible by instructions, and then eliminating the dead instructions.

With respect to original claim 9, Srivastava further discloses the limitation wherein said eliminating step further comprises determining which instruction to overwrite with reference to the pointers in the first information (see column 10, lines 1-14, which shows using the liveliness information to determine variable and register utilization and to remove dead code, and column 10, lines 28-31, which shows determining which instructions to remove).

With respect to original claim 10, although Srivastava discloses classifying entry and exit blocks in a procedure (see column 7, lines 38-46) and storing such information (see column 8,

lines 6-12), Srivastava does not expressly disclose the limitation wherein the first information associated with each exit is stored in an epilog associated with the exit, and the second information associated with each entry is stored in a prolog associated with that entry.

However, Click discloses using a register allocator to build calling convention prolog and epilog code (see the title and abstract, and column 6, lines 38-56, which shows building the prolog and epilog), in order to allow greater flexibility and faster execution (see column 6, lines 21-25). In terms of dead code elimination, the calling convention specifies how registers are to be used when procedures are called (see column 1, line 54 to column 2, line 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to store the liveliness information of Srivastava in an epilog and prolog, as taught by Click, for the purpose of allowing greater flexibility and faster execution.

With respect to amended claim 11, see the explanation for claim 1 set forth above. Note that Srivastava further discloses a computer readable medium comprising instructions (see column 3, lines 57-63).

With respect to amended claim 17, see the explanation for claim 7 set forth above.

With respect to original claim 18, see the explanation for claim 8 set forth above.

With respect to original claim 19, see the explanation for claim 9 set forth above.

With respect to original claim 20, see the explanation for claim 10 set forth above.

7. Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srivastava in view of Click as applied to claims 1 and 11 above, respectively, and further in view of U.S. Pat. No. 6,112,025 to Mulchandani et al. (hereinafter Mulchandani.

With respect to original claim 2, although Srivastava shows removing dead instructions (see column 10, lines 28-31), Srivastava does not expressly disclose the limitation wherein eliminating the dead instruction comprises overwriting the dead instruction with a NOP.

However, Mulchandani discloses replacing an instruction with a NOP in a dynamic linking system (see column 5, lines 30-37), for the purpose of preventing the unwanted effects of executing a particular instruction (see column 5, lines 42-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the dead code removal of Srivastava using the NOP replacement feature taught by Mulchandani, for the purpose of preventing the unwanted effects of executing a particular instruction.

With respect to original claim 12, see the explanation for claim 2 set forth above.

8. Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srivastava in view of Click as applied to claims 1 and 11 above, respectively, and further in view of U.S. Pat. No. 6,041,179 to Bacon et al. (hereinafter Bacon).

With respect to original claim 3, although Srivastava shows removing dead instructions (see column 10, lines 28-31), Srivastava does not expressly disclose the limitation wherein

eliminating the dead instruction comprises compacting the surrounding instructions to delete the dead instruction.

However, Bacon discloses compacting code in a program by linking only live procedures sand not including those determined to be dead (see column 11, lines 9-13), for the purpose of reducing code size.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the dead code removal of Srivastava using the code compaction feature taught by Bacon, for the purpose of reducing code size.

With respect to original claim 13, see the explanation for claim 3 set forth above.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action (the amendment changes the scope of claims 2, 3, 10, 12, 13 and 20). Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (703) 305-0352. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

Michael J. Yigdall
Examiner
Art Unit 2122

mjy
April 21, 2004

TUAN DAM
SUPERVISORY PATENT EXAMINER